REMARKS

In the Office Action mailed March 25, 2004, claim 1-18 were rejected. Claims 1-18 are pending.

In the following, the Examiner's comments are included in bold, indented type, followed by the Applicant's remarks:

> **1. Applicants has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.**

A supplemental declaration is enclosed with this Response that includes applicants' complete post office addresses.

Also, Applicants note that in the filing receipt mailed November 1, 2001, Applicant **John Elliott**'s name is misspelled as "John Elliot." Applicants respectfully request that a supplemental filing receipt be issued reflecting the correct spelling of John Elliott.

> **2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.**

Applicants request that the title of the invention be changed to "**METHODS AND PROCESSORS FOR BIT-SHIFTING MULTI-WORD VALUES.**" Applicants respectfully request that the Examiner enter this change.

Claim Rejections - 35 USC § 112

> **3. The following is a quotation of the second paragraph of 35 U.S.C. 112:**
>
> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicants regards as his invention.**

4. Claims 9-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention.

5. Claim 9 recites the limitation "the carry0 and carry 1 register" in line 6. There is insufficient antecedent basis for this limitation in the claim.

6. Claims 10-18 are rejected for incorporating the defects of claim 9.

7. Appropriate correction is required.

Applicants have amended claim 9 to clarify this limitation. Applicants submit that the limitations of claims 9-18 now have sufficient antecedent basis and respectfully request that the Examiner reconsider the rejection of claims 9-18 and that the rejection be withdrawn.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Intel's Pentium Processor Family Developer's Manual Volume 3: Architecture and Programming Manual (herein after Intel).

10. Referring to claim 1, Intel has taught a method of processing a multi-precision shift instruction, comprising:

a. fetching and decoding a multi-precision shift instruction (page 18-7, First paragraph, Instructions are inherently fetched and decoded in every processing system. Pages 4-16 and 4-17, SHLD and SHRD);

b. executing the multi-precision shift instruction on an operand within a multi-word value to shift the operand and concatenate the shifted value with bits shifted out of a previous shift operation on the same multi-word value (Pages 4-16 and 4-17, SHLD and SHRD); and

c. outputting the result (page 4-16, The result is stored back into the destination operand.).

Applicants respectfully disagree and submit that Intel does not disclose or suggest all of the limitations of claim 1. For example, in Intel's double-shift instructions, "[b]its shifted out of

the source operand fill empty bit position in the destination operand, which also is shifted." This is in contrast with "executing the multi-precision shift instruction on an operation within a multi-word value . . . and concatenat[ing] the shifted value with bets shifted out of a ***previous*** shift operation on the same multi-word value." The double-shift instructions discussed in the cited portion of Intel do not discuss operating on "bits shifted of a ***previous*** shift operation," as required by the claim.

In another example, in the cited portion of Intel, "[t]he result is stored back into the destination operand." (Intel page 4-16). This is in contrast with "outputting the result," as required by the claim. Intel's double-shift instructions, "bits [are] shifted out of the source operand [and] fill empty bit positions in the destination operand, which also is shifted." (Intel 4-16). Therefore, the result has not been output, because the result is already in the destination operand.

For these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claim 1 and that the rejection be withdrawn.

11. Referring to claim 2, Intel has taught the method according to claim 1, as described above, and further comprising storing the bits shifted out of the operand during the executing into a carry register (Pages 4-16 and 4-17, CF).

Applicants respectfully disagree and submit that Intel does not disclose or suggest all of the limitations of claim 2. First, claim 2 depends from claim 1 and for at least the reasons discussed above with regard to the independent claim is patentable over Intel. Second, the Carry Flag (CF) cited by the Examiner can store, at most, a single bit (Intel page 4-6). This is in contrast with "storing the *bits* shifted out the operand during the executing into a carry register." Therefore, the cited portion of Intel does not disclose or suggest the limitations of claim 2.

For these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claim 2 and that the rejection be withdrawn.

> **12. Referring to claim 3, Intel has taught the method according to claim 1, as described above, and wherein the multi-precision shift instruction is a shift left instruction (Page 4-16, SHLD).**
>
> **13. Referring to claim 4, Intel has taught the method according to claim 1, as described above, and wherein the multi-precision shift instruction is a shift right instruction (Pages 4-16 and 4-17, SHRD).**
>
> **For these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claim 3 and that the rejection be withdrawn.**
>
> **14. Referring to claim 6, Intel has taught the method according to claim 1, as described above, and wherein the multi-precision shift instruction specifies a shift increment (Page 4-16, The CL register or an immediate byte in the instruction specifies the number of bits to be shifted.).**
>
> **15. Referring to claim 7, Intel has taught the method according to claim 6, wherein the shift increment is greater than or equal to the number of bits in a word (Pages 4-19).**
>
> **16. Referring to claim 8, Intel has taught the method according to claim 6, as described above, and wherein the shift increment is less than the number of bits in a word (Pages 4-16, 25-289 to 25-290).**

Applicants respectfully disagree and submit that claims 3-4 and 6-8 depend from claim 1 and for at least the reasons discussed above with regard to the independent claim are patentable over Intel. Although Applicants has not provided detailed arguments with respect to claims 3-4 and 6-8, Applicants remain ready to do so if it becomes appropriate.

For these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claims 3-4 and 6-8 and that the rejections be withdrawn.

Claim Rejections - 35 USC § 103

> **17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:**
>
> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior**

> **art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**
>
> **18. Claims 5 and 9-18 are rejected under 35 U.S.C. 1 03 (a) as being unpatentable over Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel), in view of Silverbrook, VS Patent 6,314,200.**
>
> **19. Referring to claim 5, Intel has taught the method according to claim 1, as described above. Intel has not specifically taught wherein the concatenation step is performed by a logical OR operation. However, Silverbrook et al. have taught wherein the concatenation step is performed by a logical OR operation (column 222, lines 10-24) for the desirable purpose of implementing multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the concatenation step of Intel, include logical OR operation, as taught by Silverbrook et al., for the desirable purpose of implementing multiple precision shifting (column 222, lines 10-24).**

Applicants respectfully disagree. First, applicants disagree with the Examiners characterization of Intel, as discussed above. Second, Applicants note that in Silverbrook, "the bit formally known as bit 0 does not simply replace RTMP . . . . Instead, it is ***XORed*** with RTMP . . . ." (column 222, lines 20-23) Applicants note that the XOR and OR logical operations are not equivalent. Therefore, the combination of Silverbrook and Intel does not disclose or suggest all limitations of the claim.

Applicants further contend that the combination of Intel and Silverbrook is improper. The Examiner has not cited language in either reference or within information commonly known to those skilled in the art that provides the necessary motivation or suggestion to combine these two references. Applicants respectfully submit that one of ordinary skill in the art at the time of the invention would not be motivated to combine Intel and Silverbrook.

For these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claim 5 and that the rejection be withdrawn.

20. Referring to claim 9, Intel has taught a processor for processing multi-precision shift instructions, comprising:

a. a program memory for storing instructions including a multi-precision shift instruction (Page 3-2, lines 1-3);

b. a program counter for identifying current instructions for processing (Page 3-15, section 3.3.5, Instruction Pointer); and

c. a barrel shifter for executing shift instructions (Page 4-16 and 4-17), the barrel shifter including:

d. a carry register for storing values shifted out of sections of the barrel shifter (Page 4-16 and 4-17, CF); and

e. logic for concatenating values stored in the carry 0 and carry 1 registers with values in the barrel shifter (pages 25-289 to 25-292), the barrel shifter executing a shift instruction fetched from the program memory to (page 18-7, First paragraph, Pages 4-16, 4-17, 25-289 to 25-292, Page 3-2, lines 1-3) a) load an operand into a section within the barrel shifter (Pages 4-16, 4-17, 25-289 to 25-292), b) shift the operand (Pages 4-16, 4-17, 25-289 to 25-292), c) output the shifted value (Pages 4-16, 4-17, 25-289 to 25-292) and d) store into the carry register bits shifted out of the section of the barrel shifter (Pages 4-16, 4-17, 25-289 to 25-292).

21. Intel has not specifically taught all of the hardware logic required to implement the shift instructions. Intel has not specifically taught OR logic for concatenating values stored in the carry 0 and carry 1 registers with values in the barrel shifter. Silverbrook et al. have taught OR logic for concatenating values stored in the carry 0 and carry 1 registers with values in the barrel shifter (column 222, lines 10-24) in order to implement multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Intel, include the claimed OR logic, as taught by Silverbrook et al., for the desirable purpose of implementing multiple precision shifting (column 222, lines 10-24).

Applicants respectfully disagree and submit that Intel and Silverbrook do not disclose or suggest all of the limitations of claim 9. For example, in Intel's double-shift instructions, the Carry Flag (CF) cited by the Examiner can store, at most, a single bit (Intel page 4-6). This is in contrast with "a carry register for storing values shifted out of sections of the barrel shifter," as required by the claim.

In another example, as noted above, in Silverbrook, "the bit formally known as bit 0 does not simply replace RTMP . . . . Instead, it is ***XORed*** with RTMP . . . ." (column 222, lines 20-

23). The examiner has not cited any examples of "OR logic for concatenating values stored in the . . . registers with values in the barrel shifter," as required by the claim. Therefore, the combination of Intel and Silverbrook fails to disclose all limitations of claim 9. Furthermore, Applicants renew their objection to the combination of Intel and Silverbrook, as discussed above.

For these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claim 9 and that the rejection be withdrawn.

> **22. Referring to claim 10, Intel has taught the processor according to claim 9, as described above, and wherein the barrel shifter executes a multi-precision shift instruction to further e) concatenate the value in the carry register with the shifted operand prior to outputting the shifted value (pages 25-289 to 25-292).**
>
> **23. Referring to claim 11, Intel has taught the processor according to claim 9, wherein the shift instruction is a shift left instruction (Pages 4-16, 4-17, 25-289 to 25-292, SHLD).**
>
> **24. Referring to claim 12, Intel has taught the processor according to claim 9, as described above, and wherein the shift instruction is a shift right instruction (Pages 4-16, 4-17, 25-289 to 25-292, SHRD).**
>
> **25. Referring to claim 13, Intel has taught the processor according to claim 9, as described above, and wherein the shift instruction is an arithmetic shift instruction (Pages 4-13 to 4-17).**
>
> **26. Referring to claim 14, Intel has taught the processor according to claim 9, wherein the shift instruction is a logical shift instruction (Pages 4-13 to 4-17).**
>
> **27. Referring to claim 15, Intel has taught the processor according to claim 9, as described above, and wherein the shift instruction specifies a shift increment (Pages 4-16 to 4-17).**
>
> **28. Referring to claim 16, Intel has taught the processor according to claim 9, as described above, and wherein the barrel shifter executes at least two shift instructions to shift a multi-word value (Page 4-20, SHR, SHRD).**
>
> **29. Referring to claim 17, Intel has taught the processor according 16, as described above, and wherein the first instruction of the at least two shift instructions is not a multi-precision shift instruction (Page 4-20, SHR).**
>
> **30. Referring to claim 18, Intel has taught the processor according 16, as described above, and wherein the second and subsequent instructions of the at least two shift instructions is a multi-precision shift instruction (Page 4-20, SHRD).**

Applicants respectfully disagree and submit that claims 10-18 depend from claim 9 and for at least the reasons discussed above with regard to the independent claim are patentable over Intel and Silverbrook. Although Applicants has not provided detailed arguments with respect to claims 10-18, Applicants remain ready to do so if it becomes appropriate.

For these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claims 10-18 and that the rejections be withdrawn.

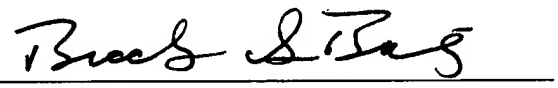
Information Disclosure Statement

Applicants note that the Examiner's list of references excluded all references listed in the Information Disclosure Statement filed by Applicants on June 1, 2001. A duplicate copy of the correspondence, including the canceled receipt postcard is enclosed. Applicants request that the Examiner review the cited references and initial the Information Disclosure statements.

SUMMARY

Applicants contend that the claims are in condition for allowance, which action is requested. Applicants do not believe that any fees are necessary with this response. Should any fees be required, Applicants requests that the fees be debited from deposit account number 50-1673.

Respectfully submitted,



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Date: June 25, 2004